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8-2302

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Atty. Docket

KARL J. WOOD ET AL

PHGB 010035

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Group Art Unit: 2613

Filed: FEBRUARY 15, 2002

Title: APPARATUS

Commissioner for Patents
Washington, D.C. 20231

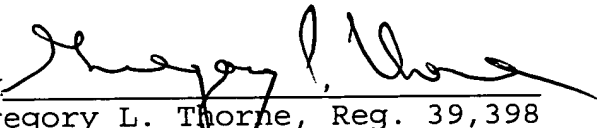
LETTER TO OFFICIAL DRAFTSMAN

Sir:

Enclosed are (2) TWO sheets of formal drawings
for filing in the above-identified application.

Respectfully submitted,

By


Gregory L. Thorne, Reg. 39,398
Senior Patent Counsel
(914) 333-9665

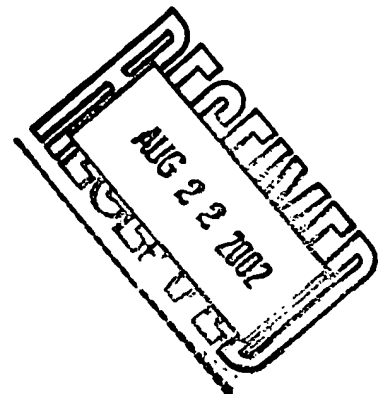
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On August 6, 2002

By Neemi Chape



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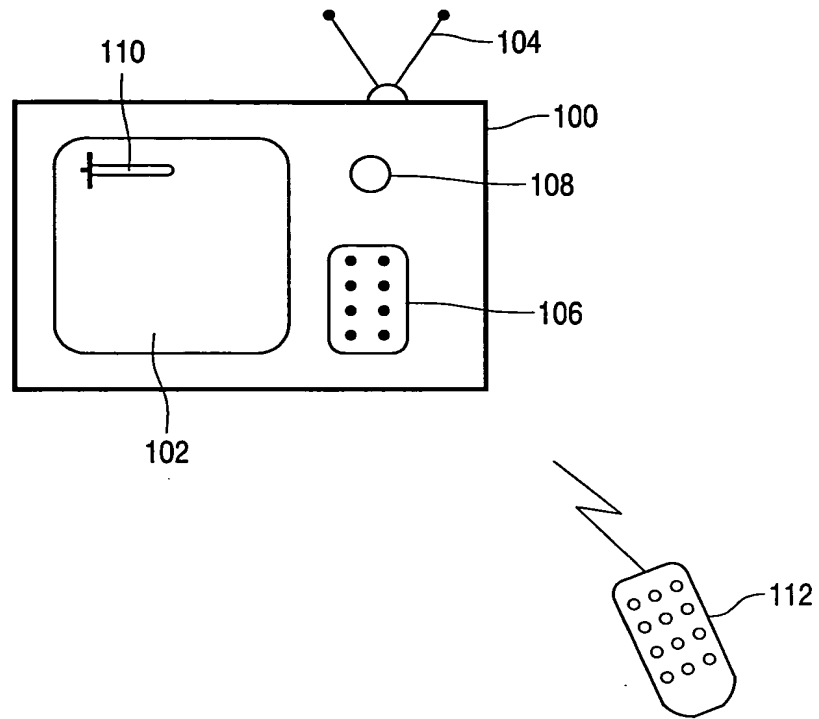


FIG. 1

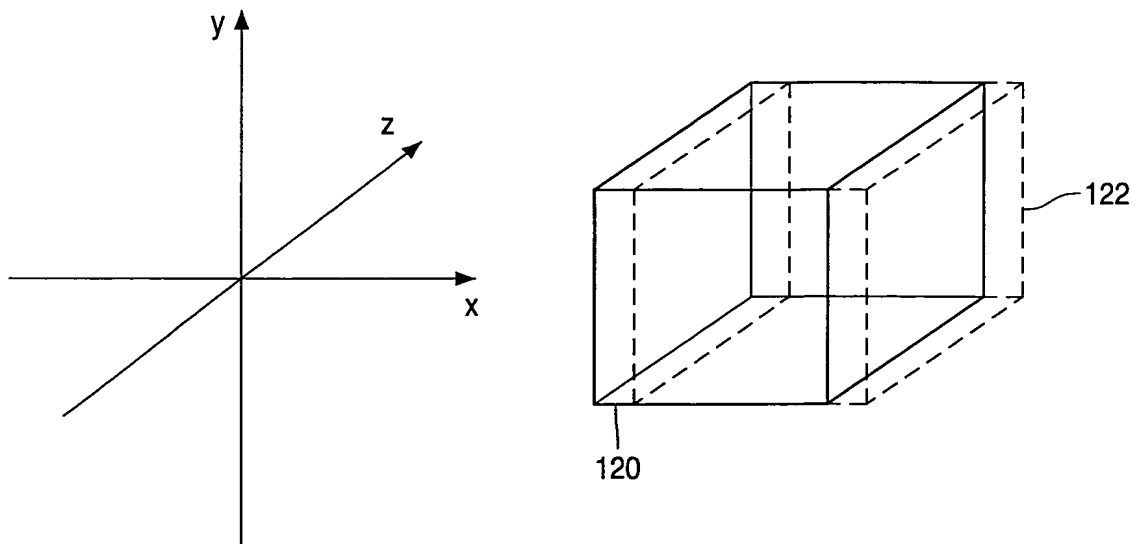


FIG. 2

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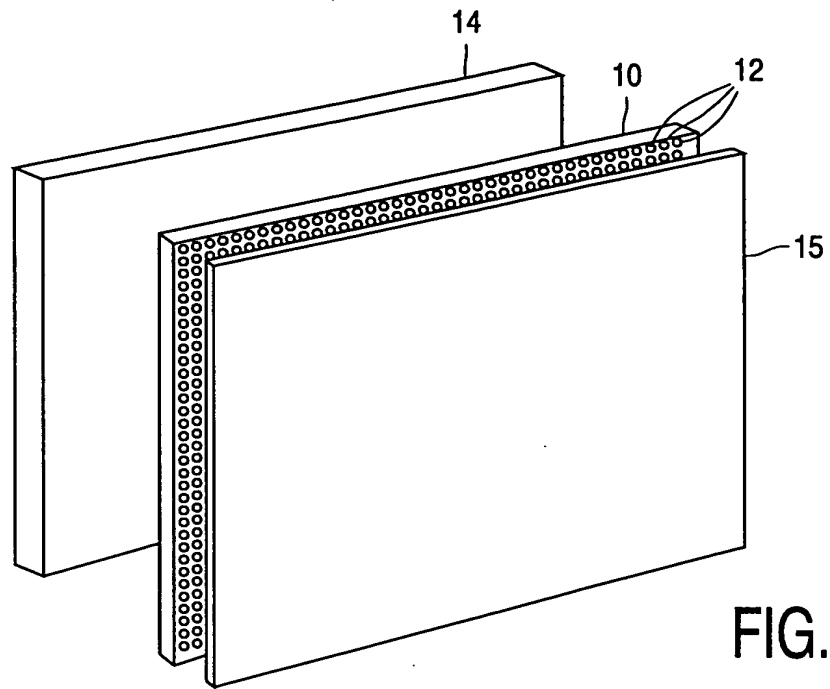


FIG. 3

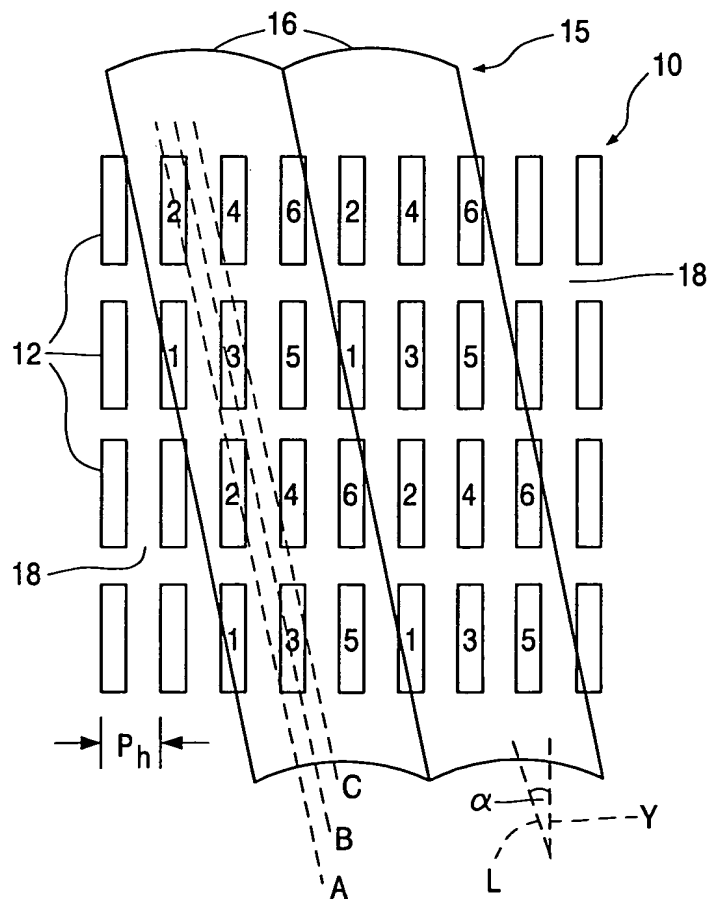


FIG. 4



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Link
1 — Design

Communication Link
Requirements



Bit Error Rate
Performance Estimation

Algorithm
2 — Design

subsystem model
descriptions



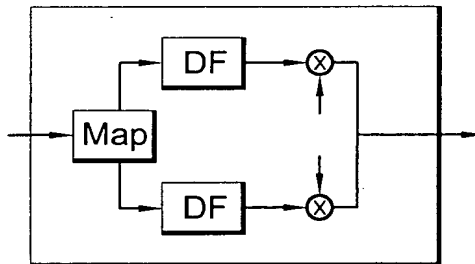
Acquisition Performance
Tracking Stability
Spectral Properties
Multiaccess



Architecture
3 — Design



Active Area Throughput
Estimated Power
Estimated Timing
Bittrue behavior



Circuit
4 — Design



Power
Routing Capacitance
Netlist Errors

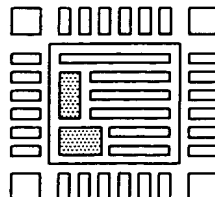


FIG. 1A



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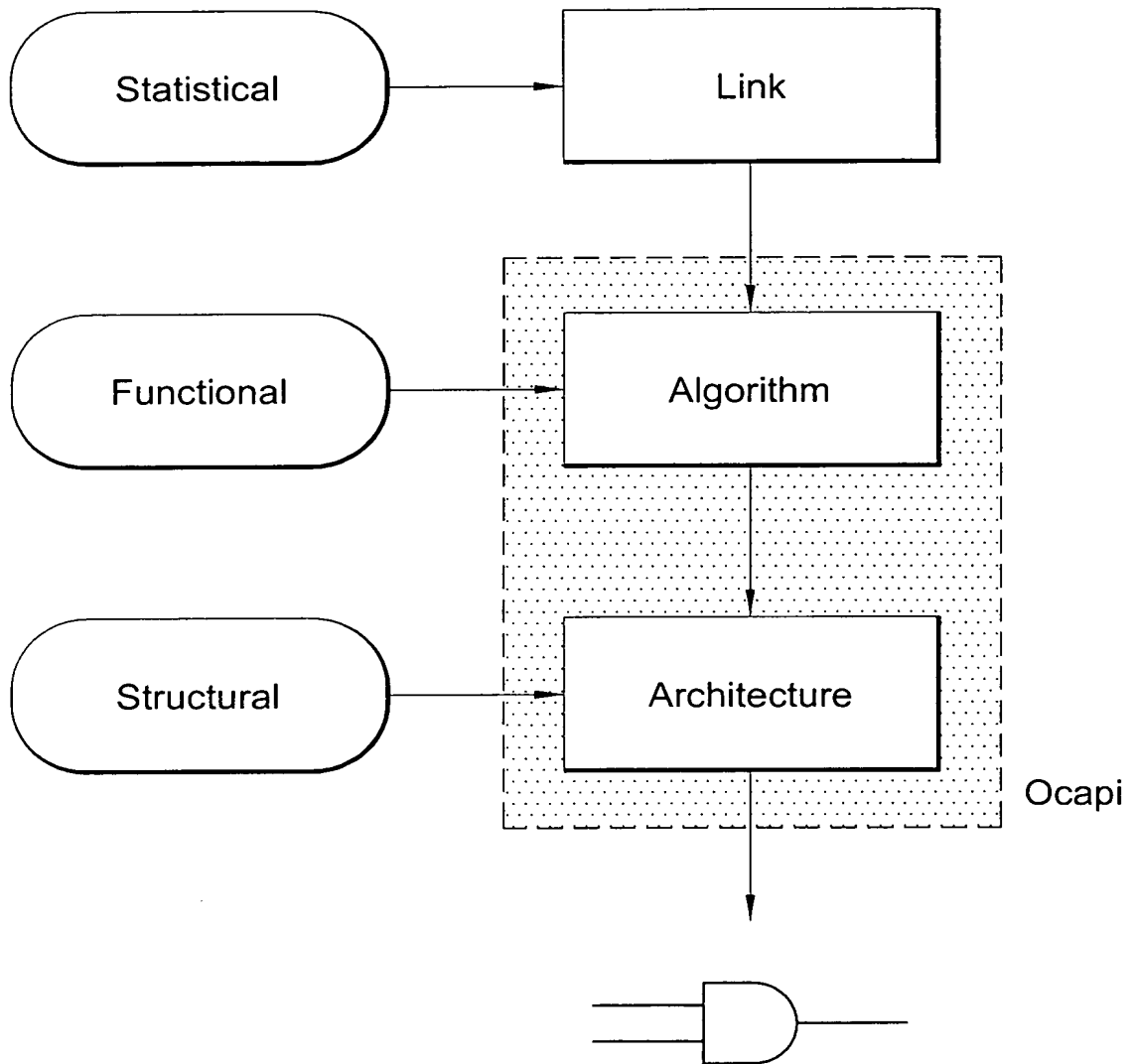


FIG. 1B



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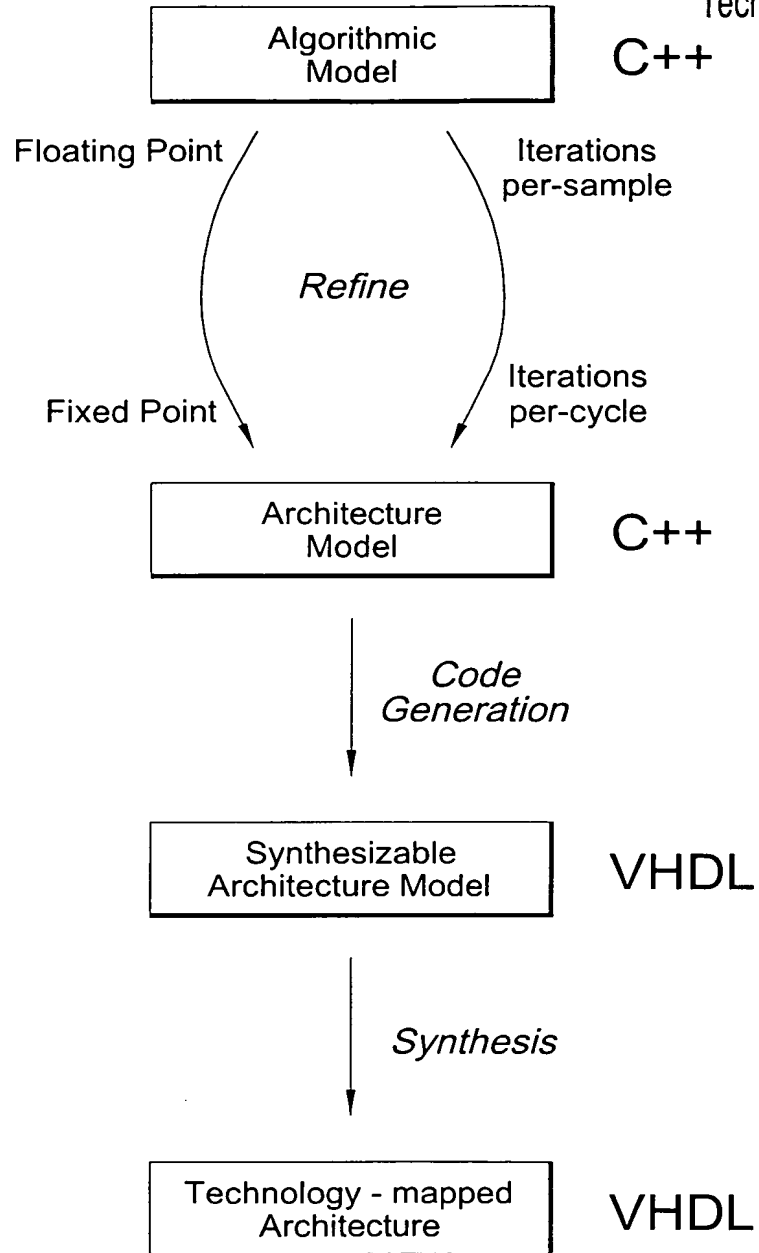


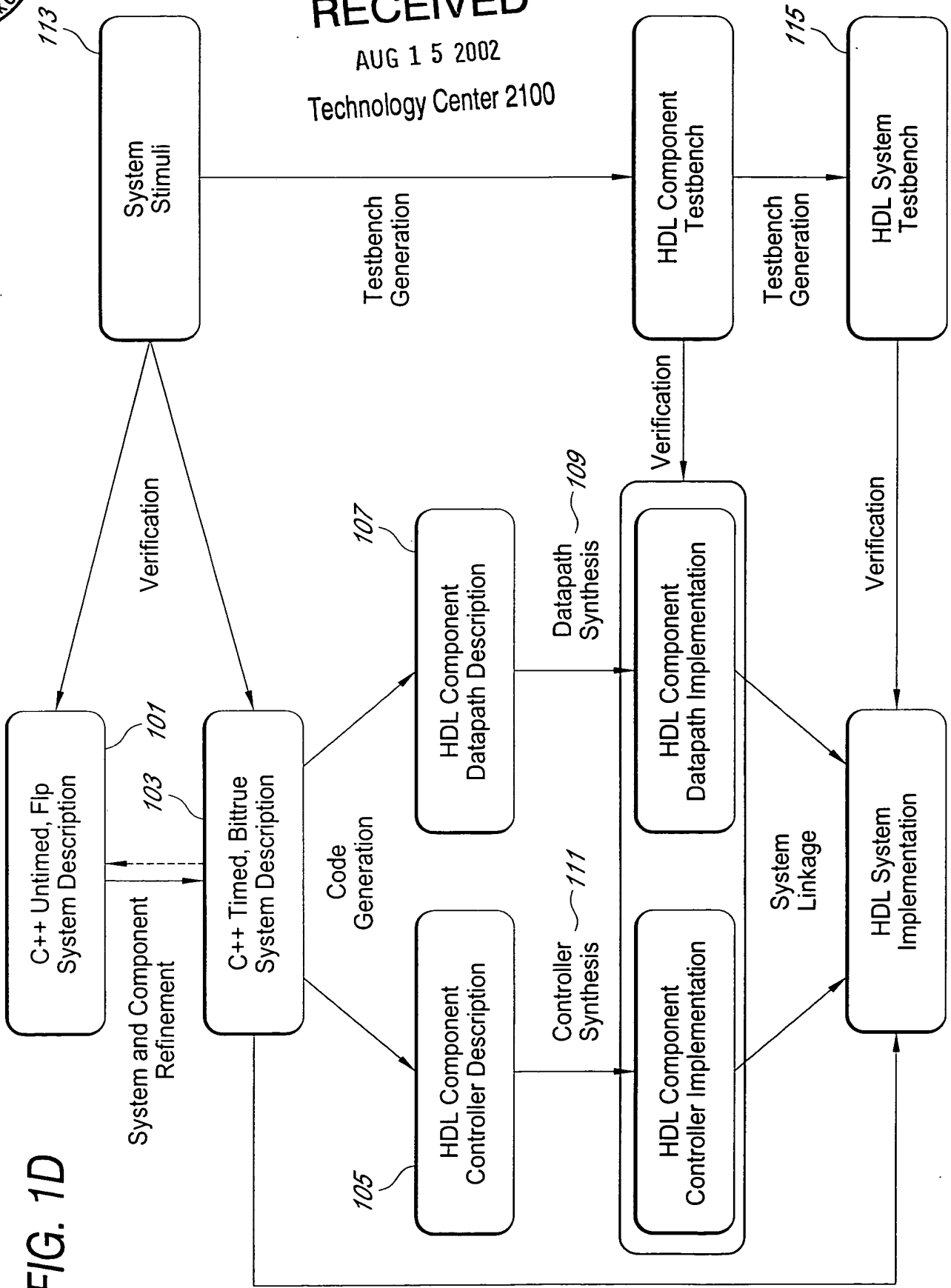
FIG. 1C



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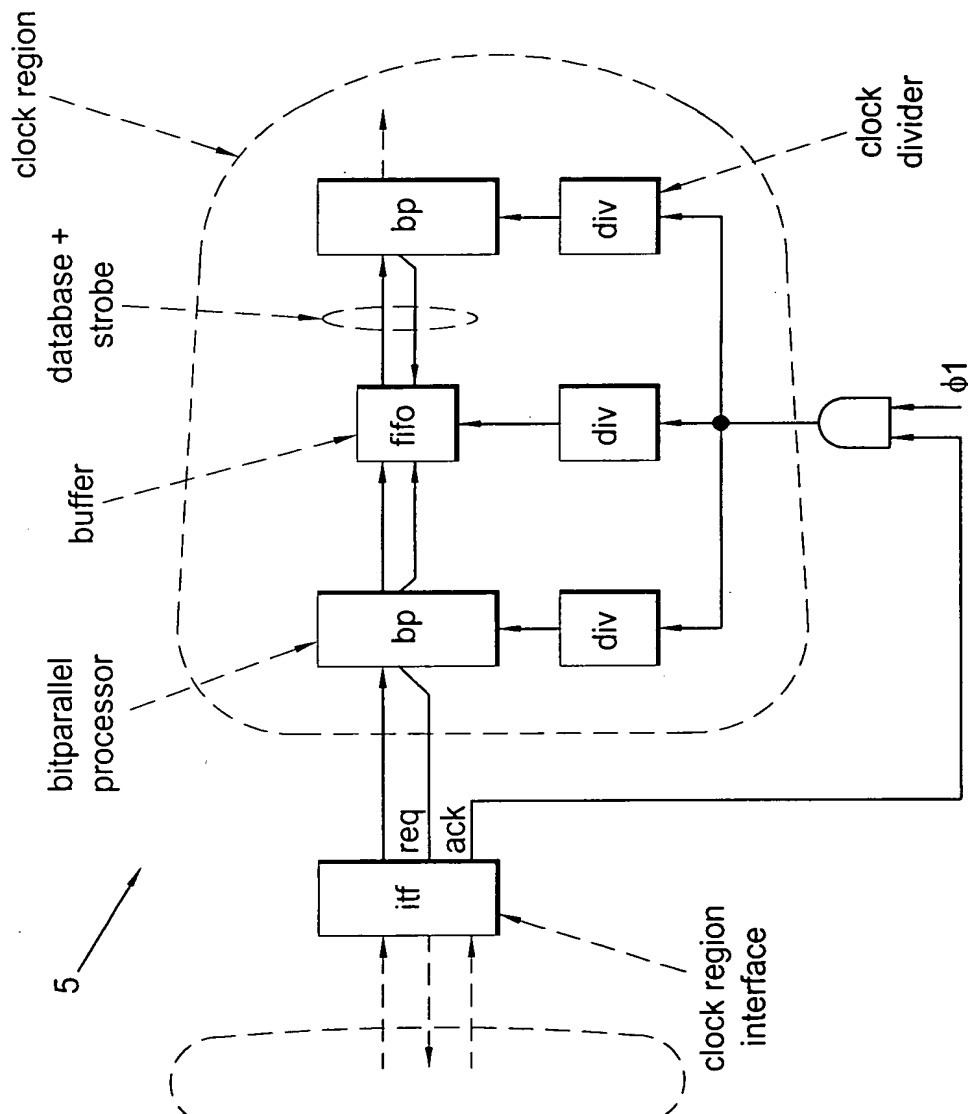


FIG. 2



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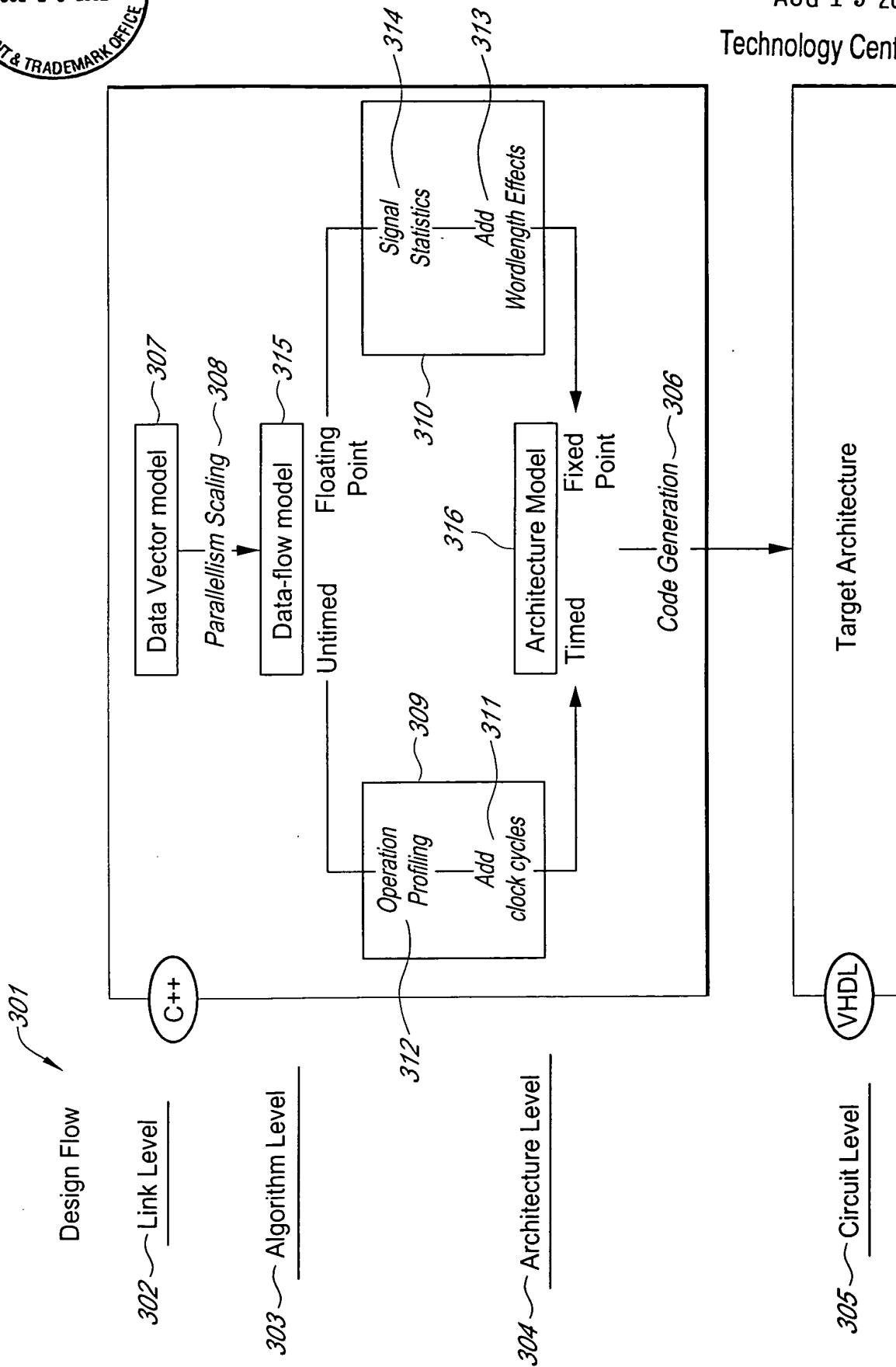


FIG. 3



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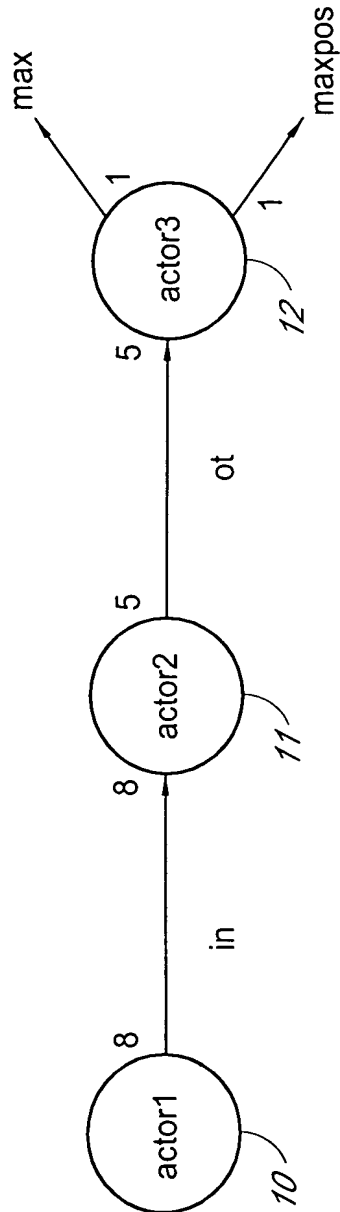


FIG. 4

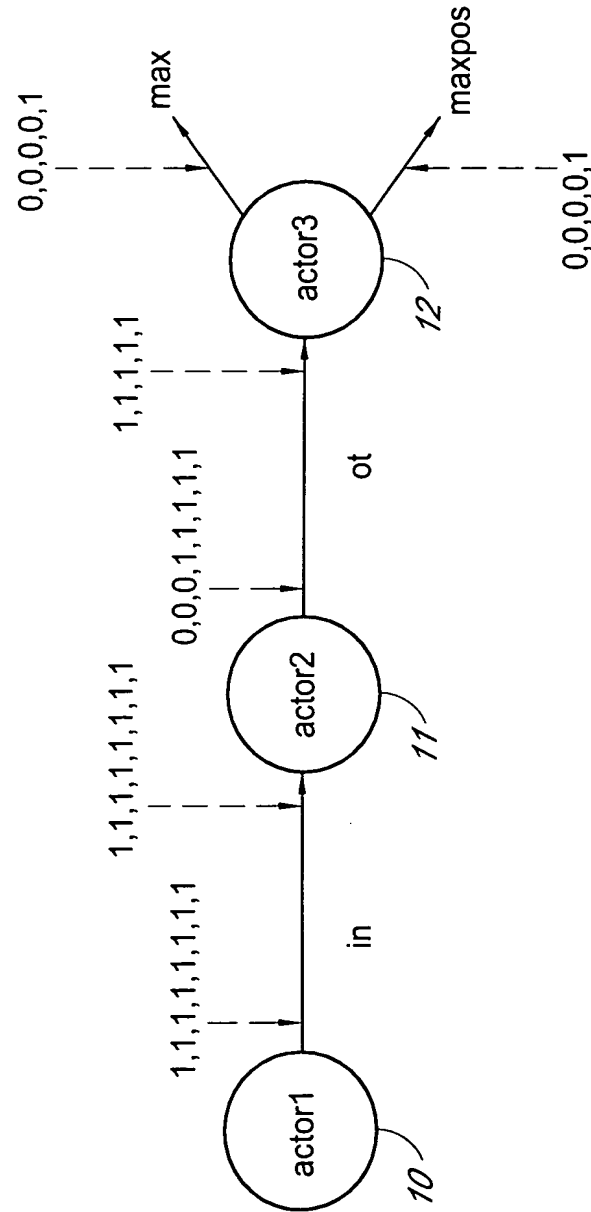


FIG. 5



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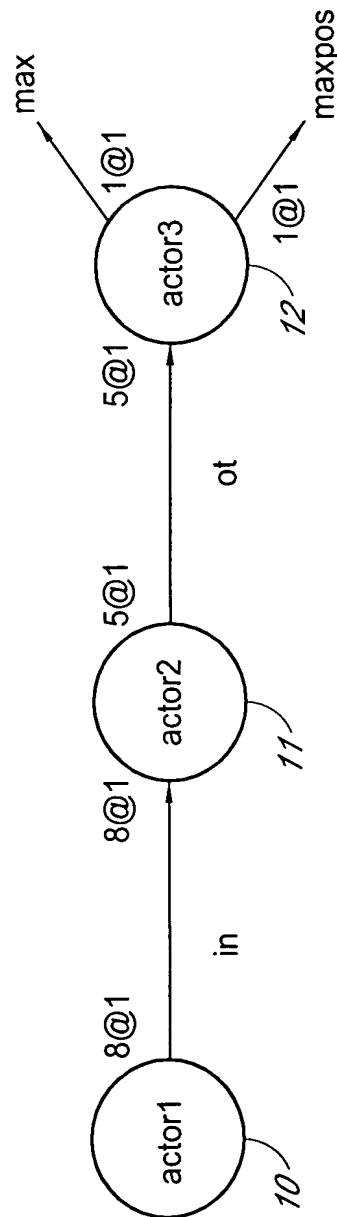


FIG. 6



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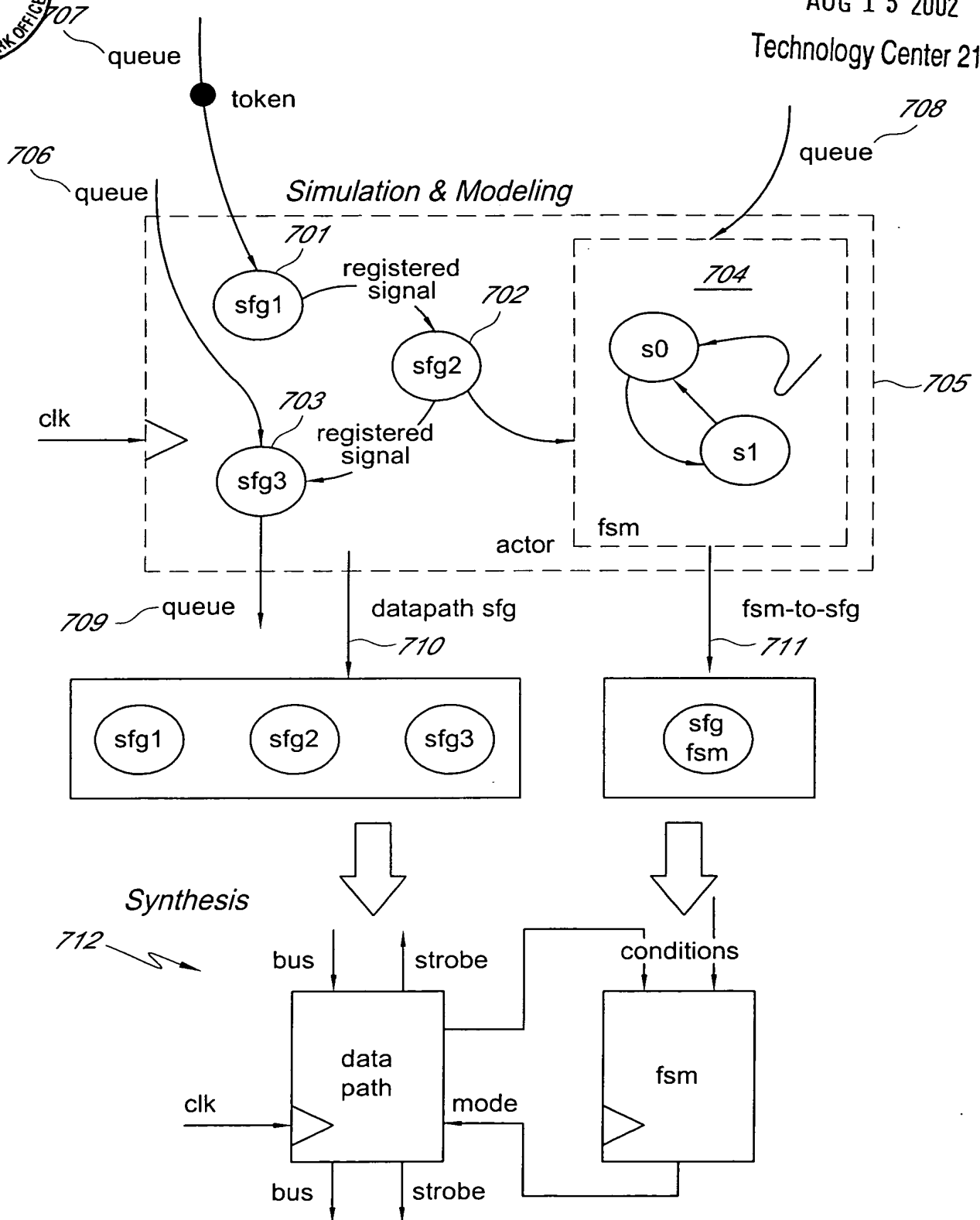


FIG. 7



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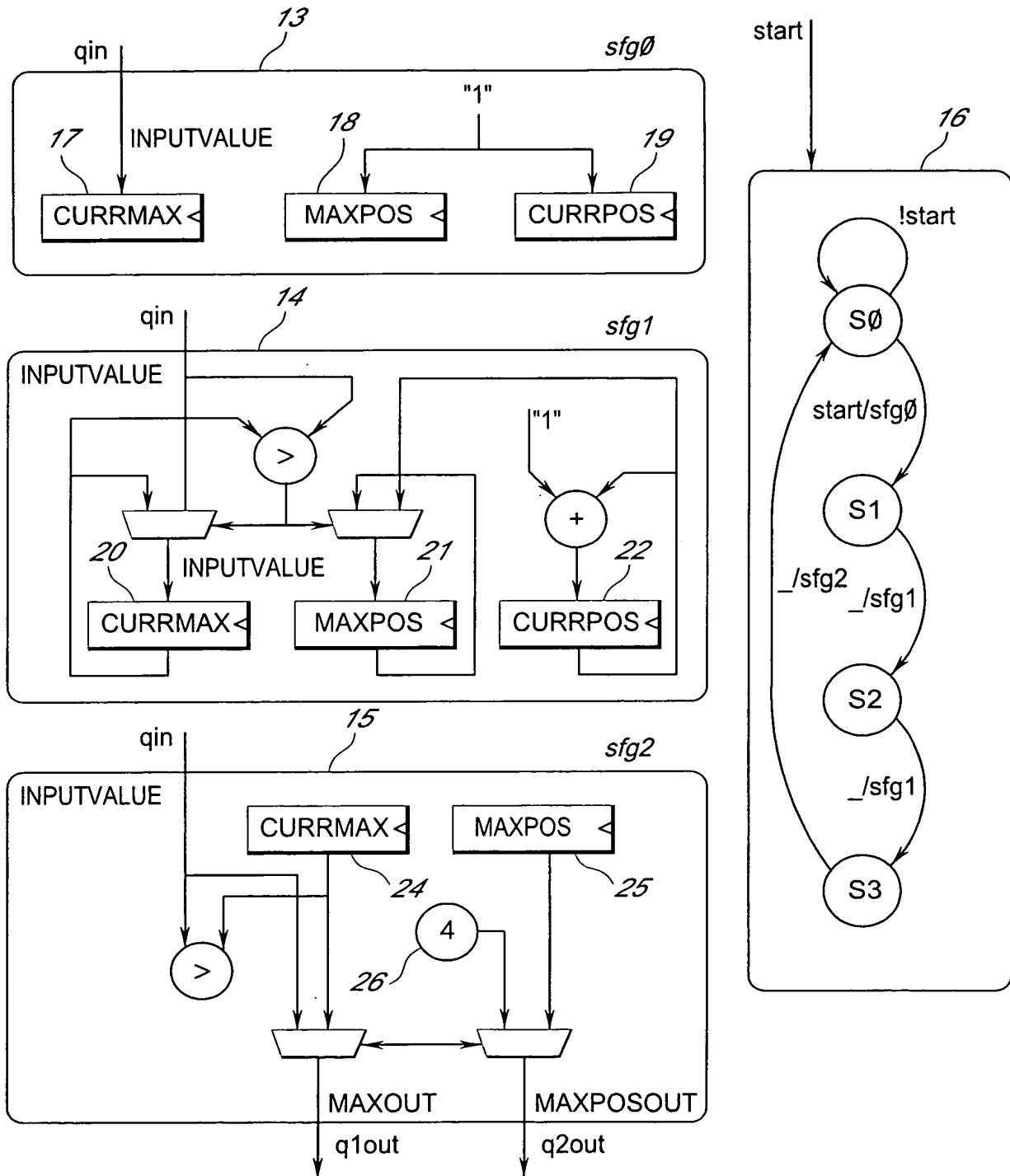


FIG. 8



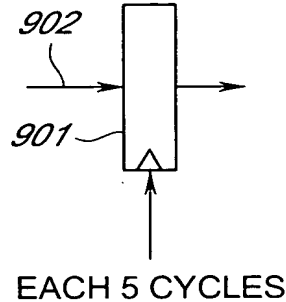
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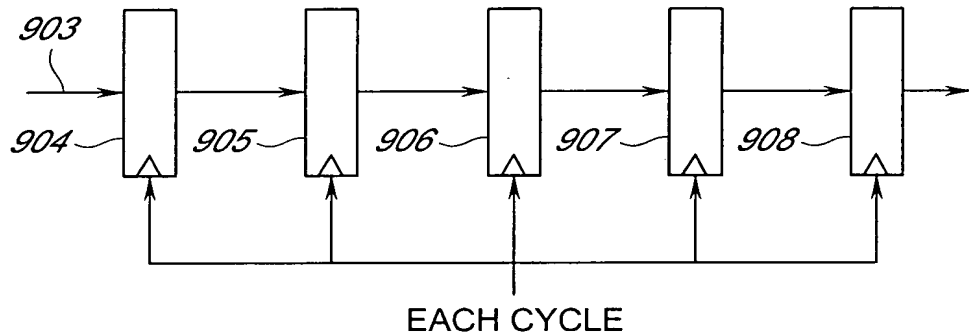
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TOKEN CONCURRENCY=1
TOKEN LATENCY=5

FIG. 9A



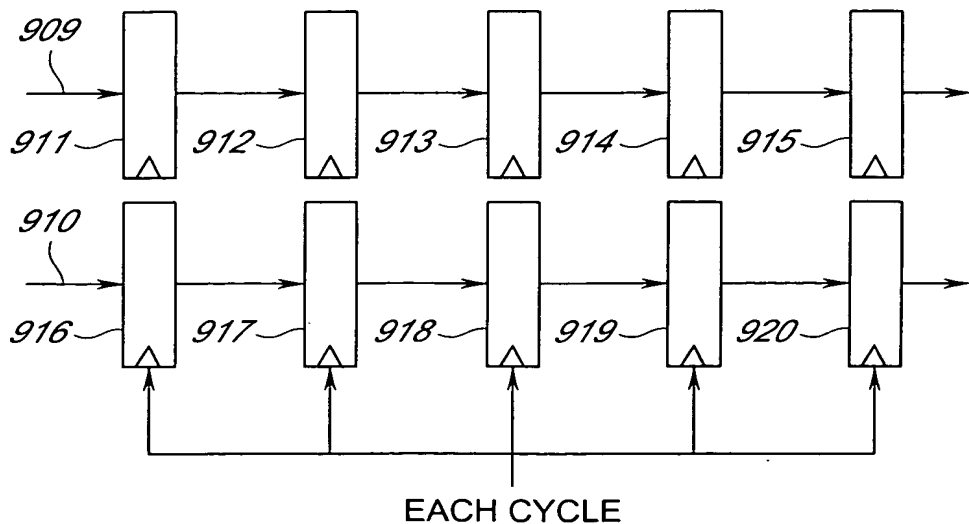
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TOKEN CONCURRENCY=1
TOKEN LATENCY=1

FIG. 9B



TRAVEL DELAY=5
TOKEN CONCURRENCY=2
TOKEN LATENCY=1

FIG. 9C



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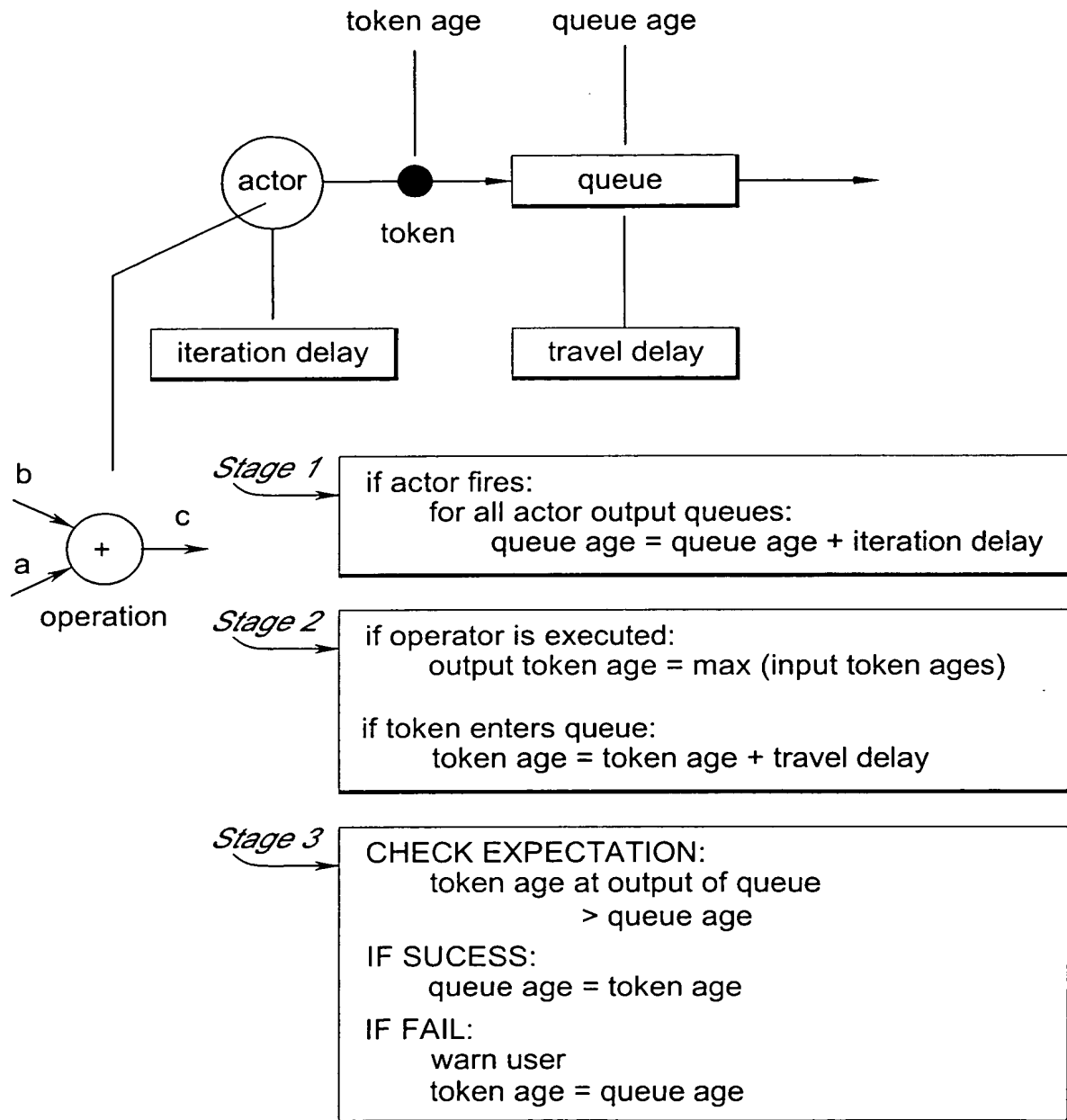


FIG. 10



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```
dfix T_sample(8, 6);
dfix T_acc (8, 6);
dfix T_bit (1, 0, ns);
double hardwired_coef = { 0.5, 0.2, -0.3, 0.15 };
```

```
fsm correlator: :define(clk & _ck)
{
```

```
    sig_array coef      (4, ck, T_sample);
    sig_array sample    (4, ck, T_sample);
    sig      accu       (ck, T_accu);
    sig      sample_in  (T_sample);
    sig      coef_in    (T_sample);
    sig      corr_out   (T_sample);
    sig      load       (ck, T_bit);
    sig      load_ctr   (T_bit);
```

FIG. 11

```
    sfg initialize_coefs;
    for (i = 0; i < 4; i++)
        coef[i] = W(T_sample, hardwired_coef[i]);
```

```
    sfg load_coef_0;
    input(coef_in);
    coef[0] = in_coef_in;
```

```
    sfg correl_1;
    accu = cast(T_acc, coef[0] * sample[0] + coef[1] * sample[1]);
```

```
    sfg correl_2;
    corr = accu + cast(T_acc, coef[2] * sample[2] + coef[3] * sample[3]);
    output(corr);
```

```
    sfg read_sample;
    input(sample_in);
    for (i = 3; i >= 0; i--)
        if (i)
            sample[i] = sample[i-1];
        else
            sample[i] = sample_in;
```

```
    sfg read_control;
    input(load_ctr);
    load = load_ctr;
```

```
    fsm myfsm;
    initial rst;
    state phase_1
    state phase_2
    rst << always << initialize_coefs << phase1;
    phase1 << always << read_control << phase2;
    phase2 << !cnd(load) << correl_1 << phase2;
    phase2 << cnd(load) << read_sample << phase1;
    phase2 << cnd(load) << correl_2 << phase1;
    phase2 << cnd(load) << read_sample << phase1;
    phase2 << cnd(load) << load_coef_0 << phase1;

    return mysfm;
}
```


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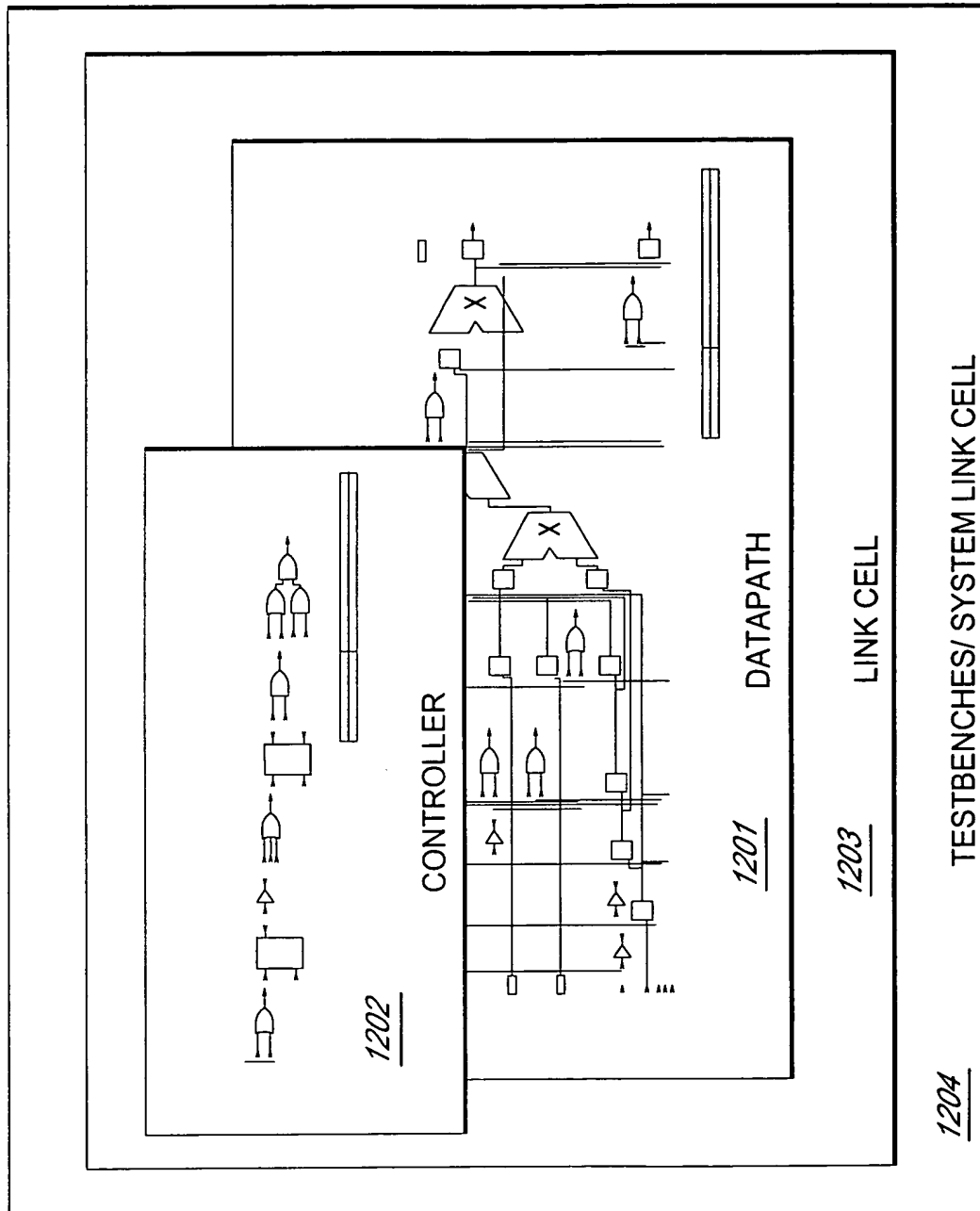


FIG. 12



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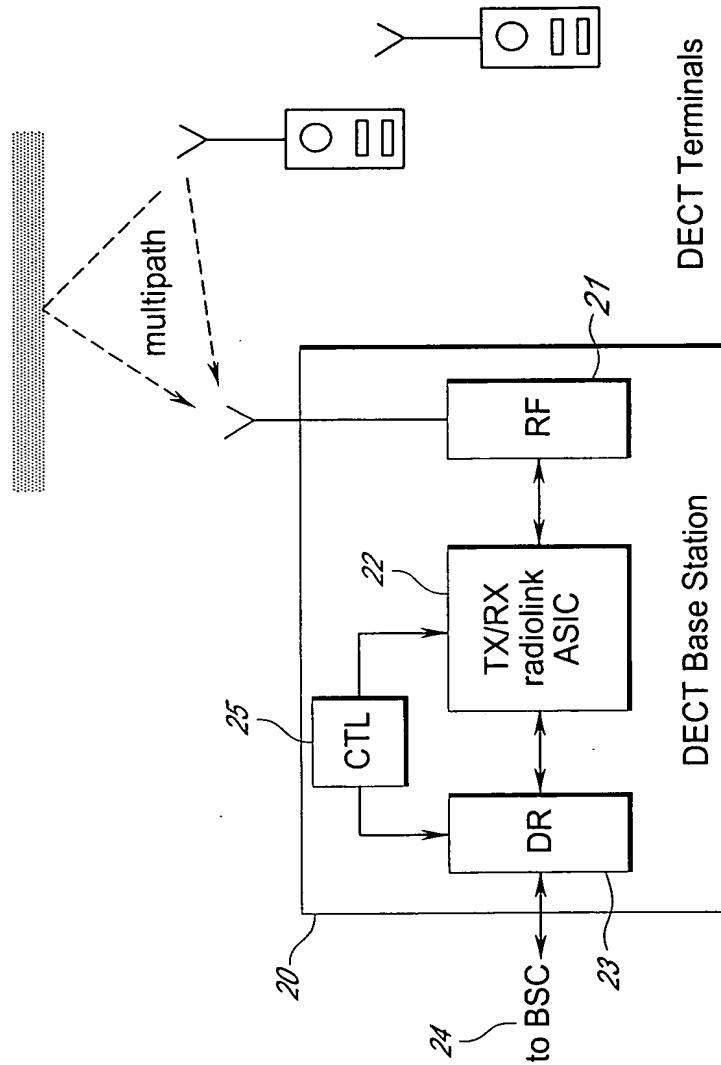


FIG. 13

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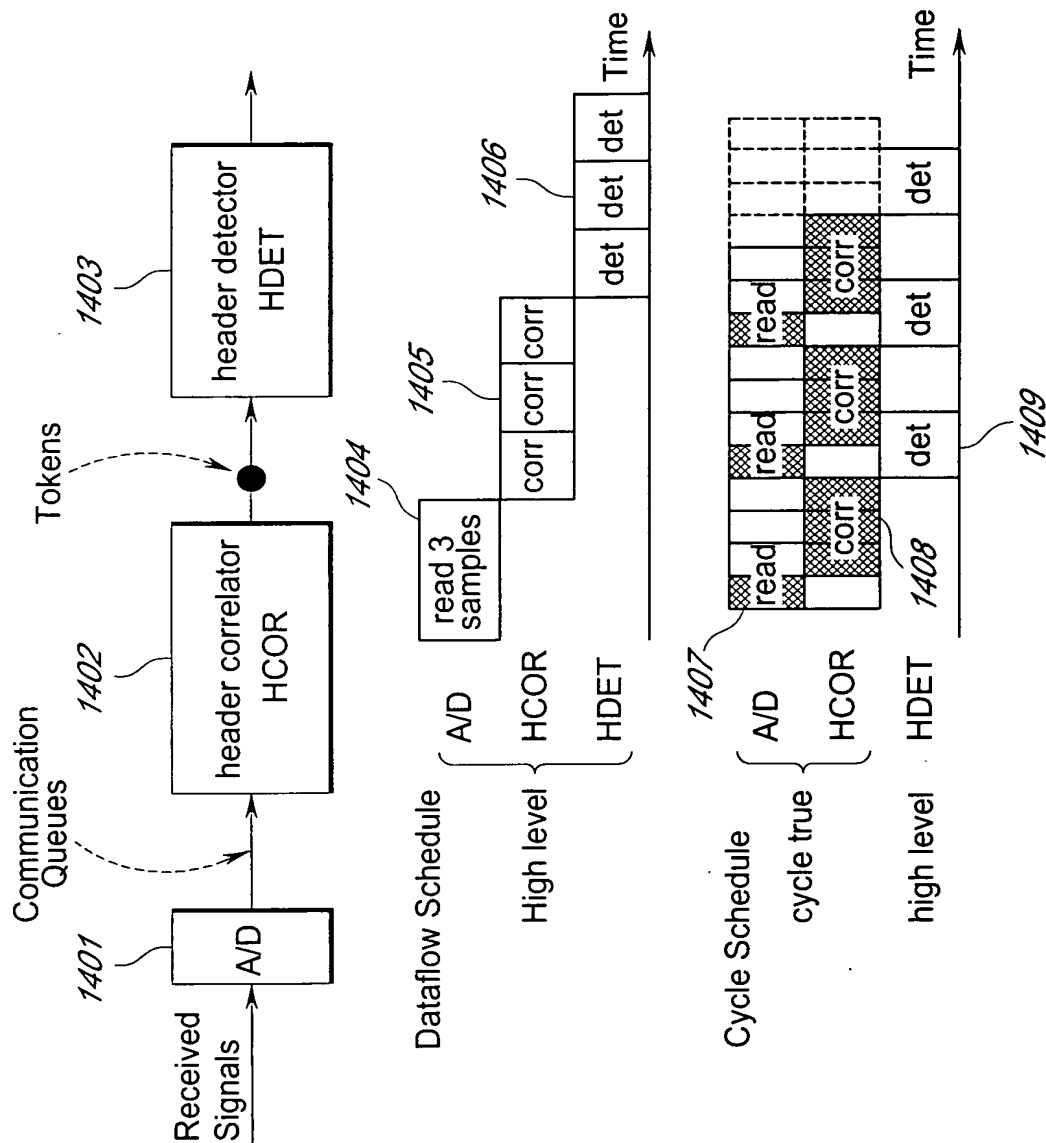


FIG. 14



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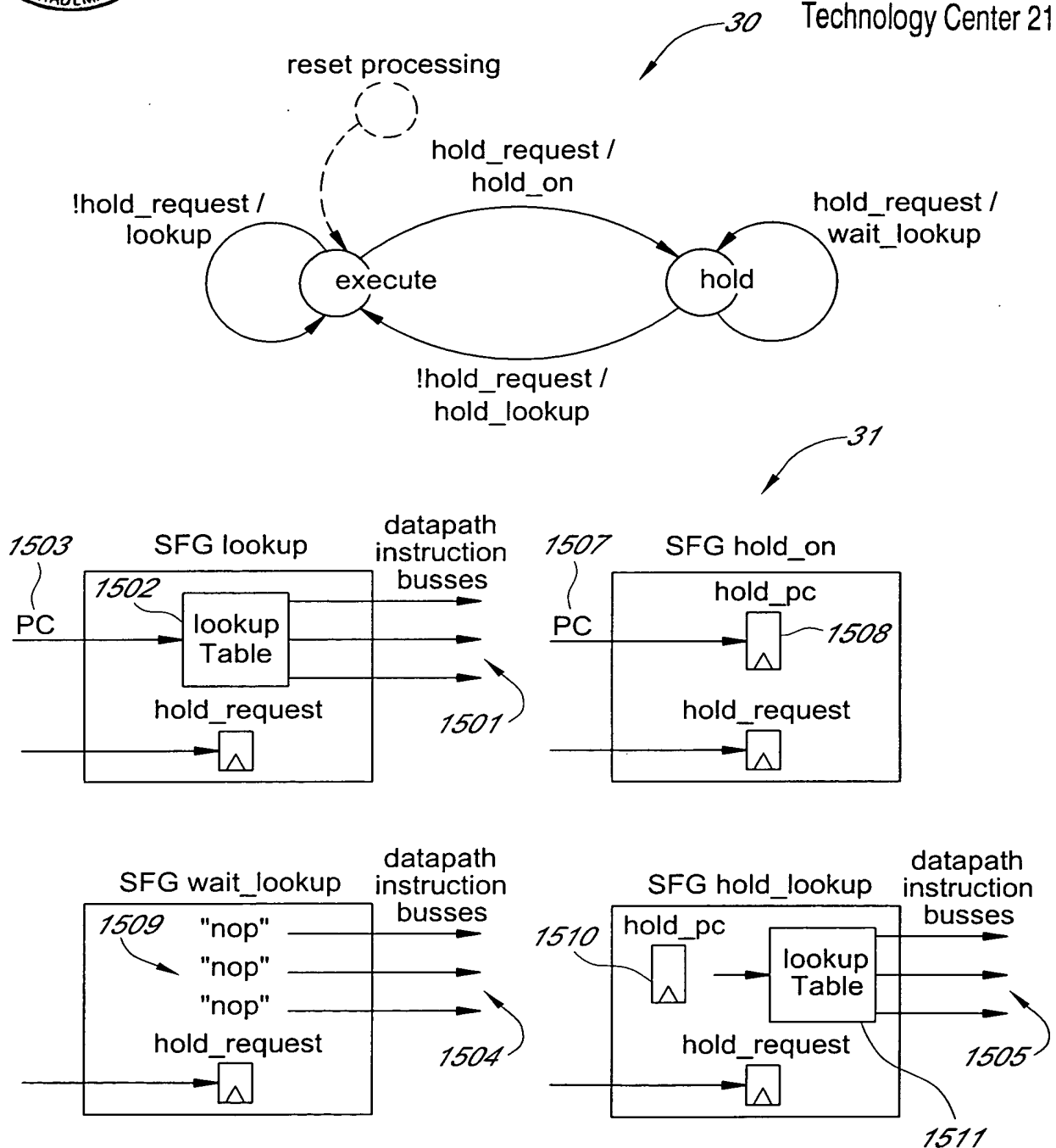


FIG. 15

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Sig Class

```

class sig {
    Value value;
    char *name;
public:
    sig(value v);
    sig operator + (sig v);
    virtual Value simulate ();
    virtual void gen_code (ostream &os);
};

sig sig: :operator + (sig v) {
    sigadd s;
    add.left = &v;
    add.right = this;
    return add;
}

Value sig: :simulate() {
    return value;
}

sig: :gen_code (ostream &os) {
    os << name;
}

```

**Derived Operator Class**

```

class sigadd : public sig {
    sig *left;
    sig *right;
public:
    Value simulate();
    void gen_code (ostream &os);
};

Value sigadd: :simulate() {
    return left->eval() +
           right->eval();
}

sigadd: :gen_code (ostream & os) {
    os << left->cg()
       << " + "
       << right->cg();
}

```

FIG. 16



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sig a, b, c, d;
b = a + 3;
d = (b + c) << 3;

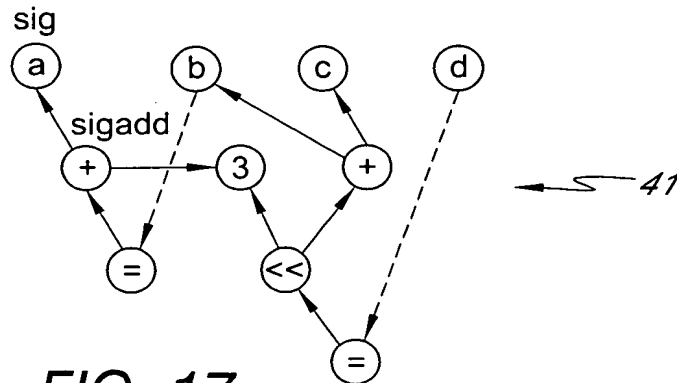
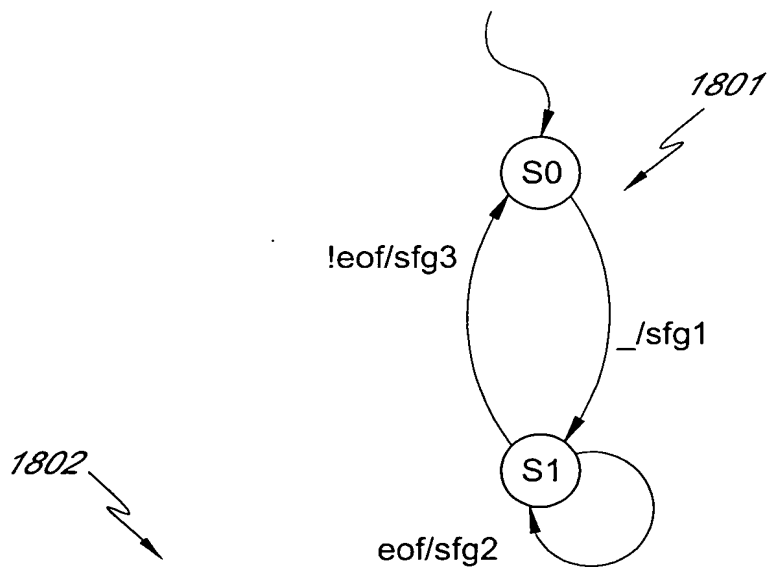


FIG. 17



fsm f;
initial s0;
state s1;

s0 << allways	<< sfg1 << s1;
s1 << cnd.eof)	<< sfg2 << s1;
s1 << !cnd.eof)	<< sfg3 << s0;

FIG. 18



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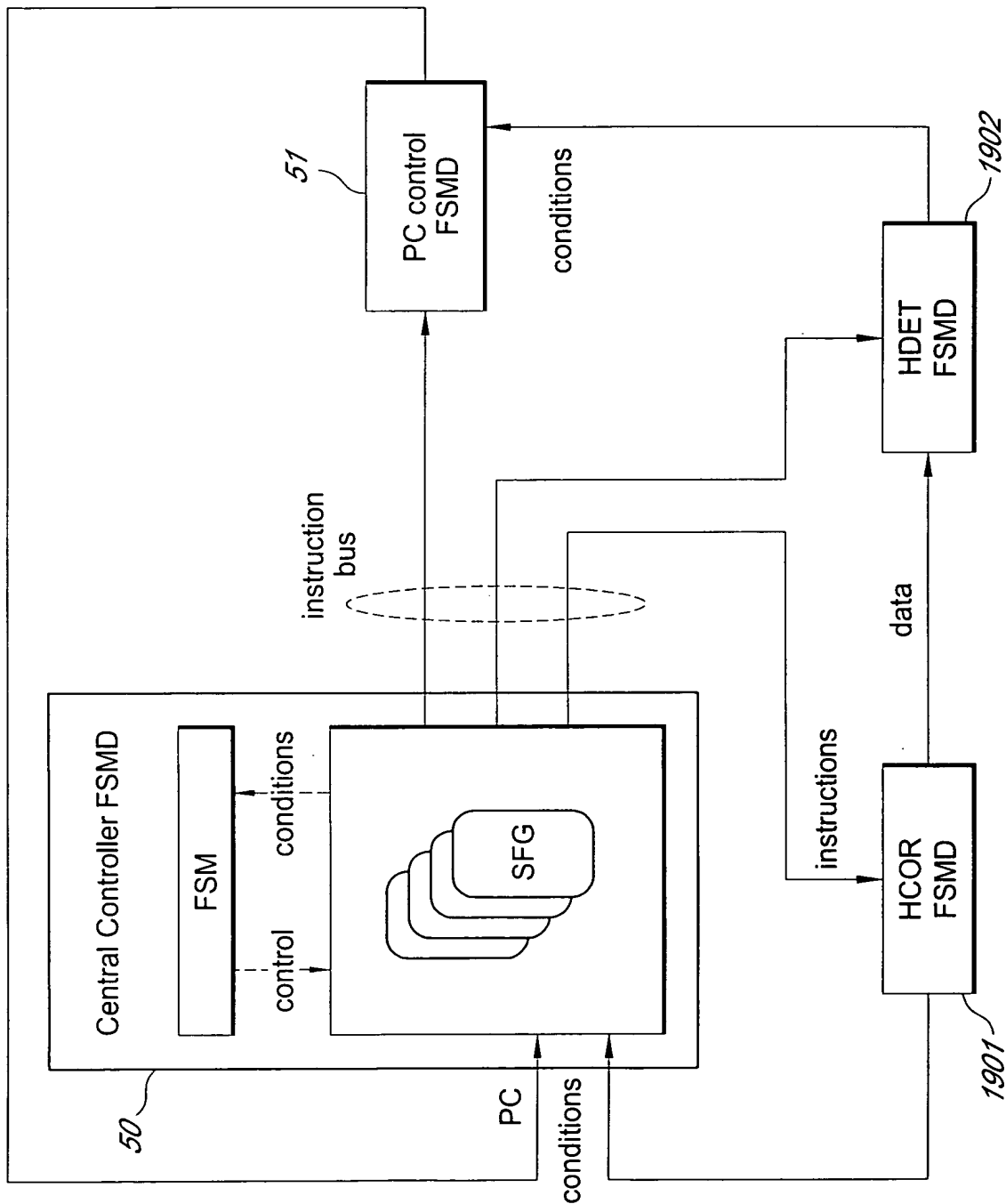


FIG. 19



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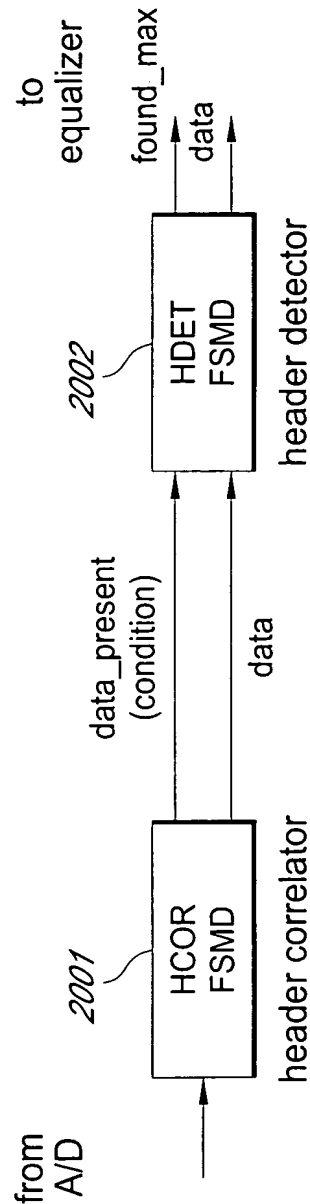


FIG. 20



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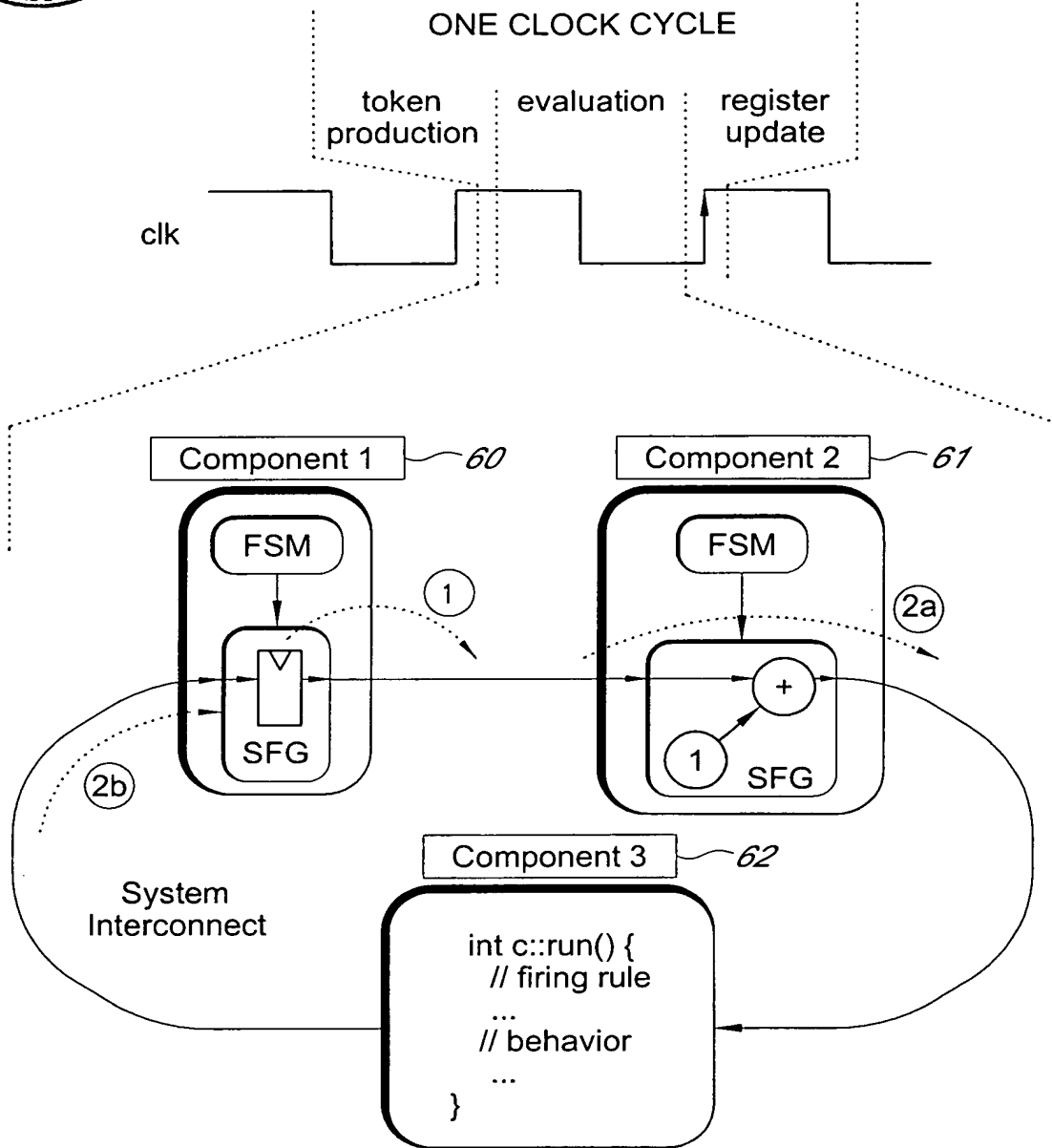


FIG. 21



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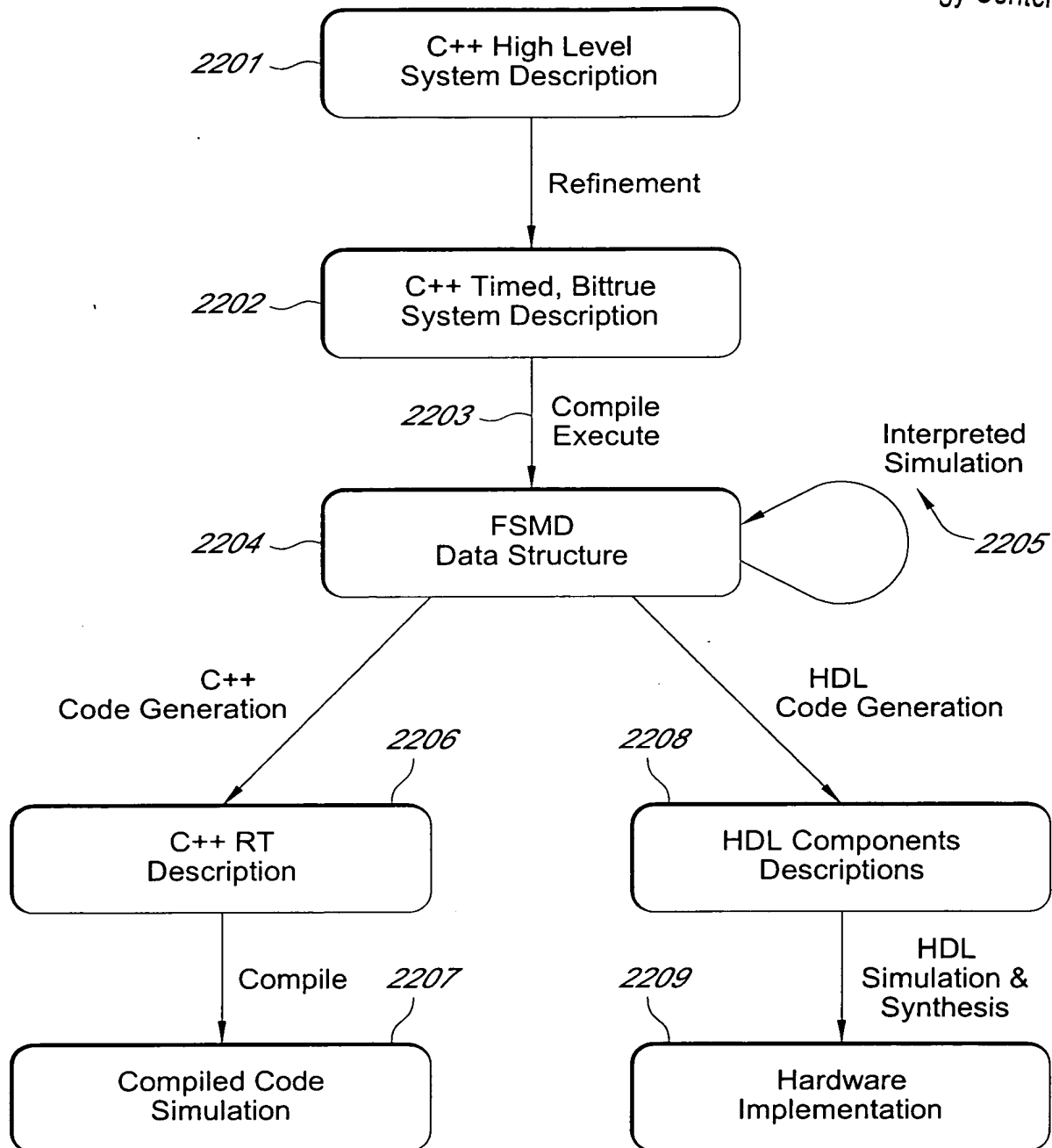


FIG. 22

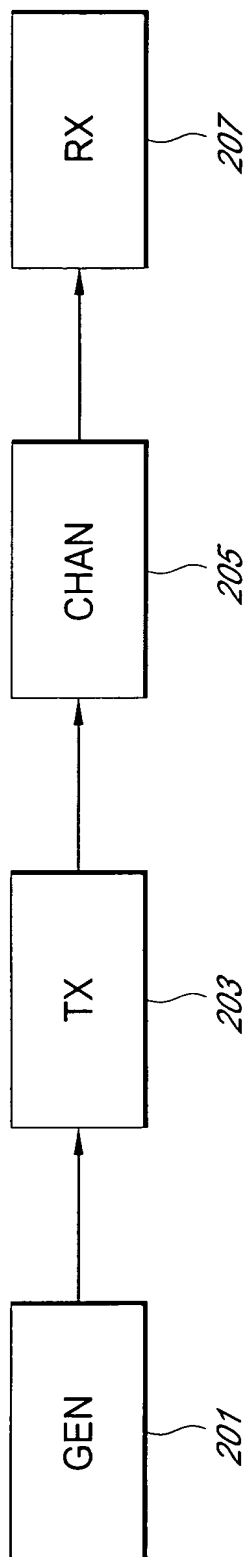


FIG. 23

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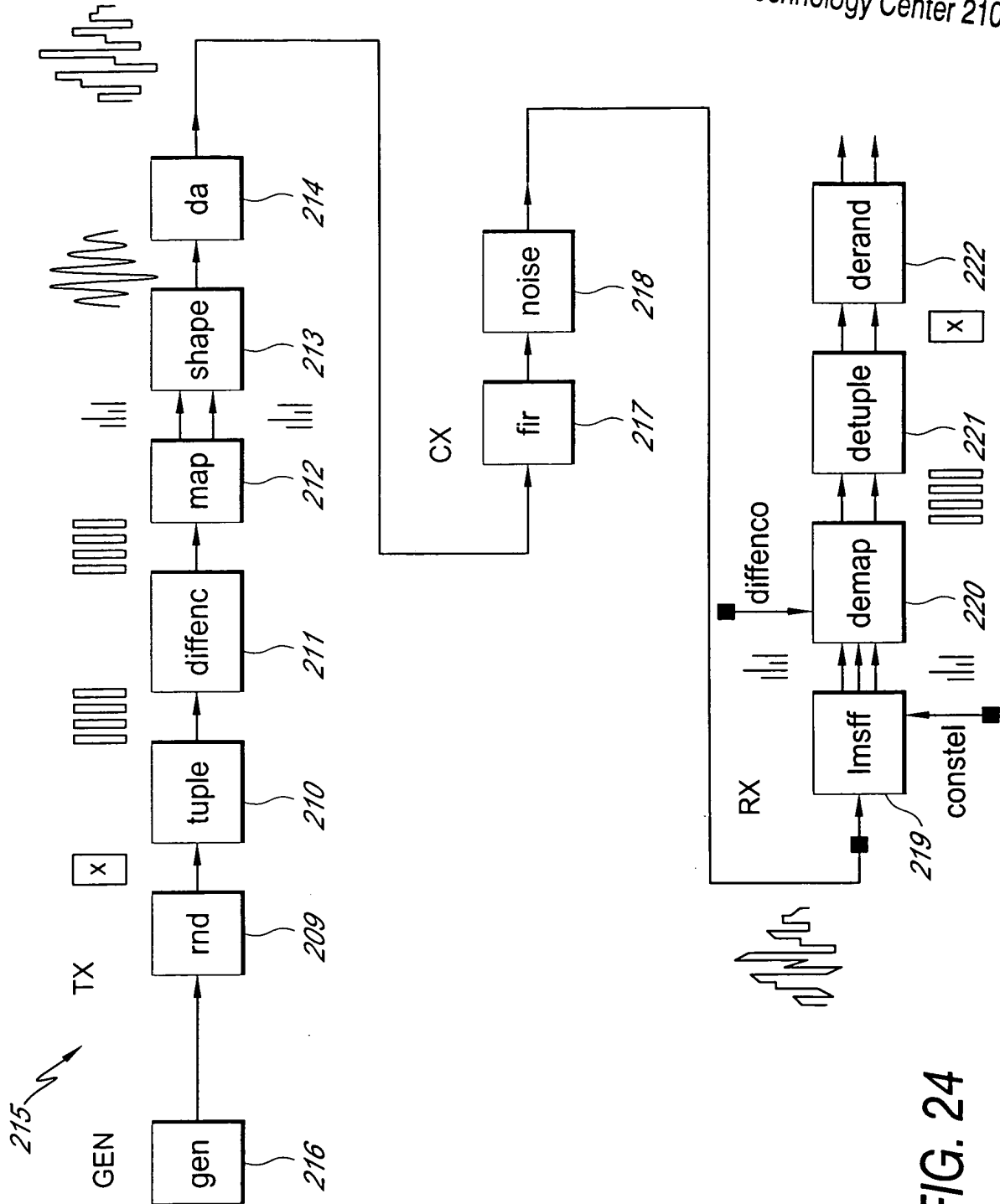


FIG. 24